Single-phase multilevel inverter topologies based IM Drive with self-voltage balancing capabilities

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Abstract — **In this paper, a new single-phase multilevel inverter topology is proposed for induction motor speed control with a battery as a source. The battery voltage will be stepped up using the boost converter and provided to the multi-level inverter. A control circuit is used in order to control the dc voltage which in turn controls the motor speed. The proposed inverter provides 9 level ac output with less number of switches, capacitors, and dc voltage sources which leads to a reduction in cost and also size of the inverter. In this, the capacitor voltage can be balanced naturally using the switching sequence of the inverter without the aid of any capacitor voltage control strategy. The proposed system is simulated in MATLAB/Simulink software.**

Key words— **Electric Vehicle, Induction motor drive, Boost Converter, Voltage mode controller. capacitor voltage balancing.**

1. Introduction

Various topologies of multilevel inverters (MLI) are used in order to overcome the limitations of restriction in voltages in the conventional 2-level voltage source inverter and to achieve the increase in power level by arranging series connection of power electronic devices using suitable control strategies. Since the MLIs are introduced, it is adapted in high power applications like renewable energy sources, AC drives active filters, etc. The MLIs also provides improvement in power quality, reduced switch voltage stress, THD and losses. The well-known topologies of multi-level inverters are flying capacitor (FC), Cascaded H-Bridge (CHB), Neutral point clamped (NPC) needs more number of power electronic components along with the respective auxiliary components such as driver circuit components, heat sinks and voltage sources which causes increase in complexity, cost, space and minimizes the efficiency in the system. The challenge here is to increase the number of levels without adding more components or reducing it. A MLI topology was proposed in the cascaded configuration, however the requirement of bi directional power electronic switches results in increase in losses. Also, it operates in symmetrical voltage sources only.

The balancing of power between different voltage sources is hard to achieve and results in reduction in the life. A cascaded structure is proposed but as it needs more bidirectional switches which causes increase in power losses. Also, the switch voltages are equal to input voltage, the stresses on the switch are higher. Hence for more number of voltage levels, it is not suitable. A new MLI topology with less number of switches is proposed and the switching losses are also greatly reduced. But due to absence of modular feature, the number of levels cannot be extended further. Moreover, the loads supplied by these MLI topologies should be near to the unity power factor. Another two MLI topologies are proposed based on H-Bridge structure but it needs individual dc voltage sources which results in increase in cost. The multiple dc sources are replaced with capacitors having dc voltage source connected in parallel to the capacitors. In these four power electronic switches have voltage stress across them same as input voltage. As the sub blocks are connected in cascaded structure, it can be used for high voltage applications. This can be used for asymmetrical voltage sources also and the maximum number of voltage levels are also achieved. The capacitor voltages are controlled by introducing a new modulation strategy using phase shifting. A four-leg inverter of NPC structure is proposed with selective harmonic elimination/mitigation strategy and it also balances the capacitor voltages even at minimum switching frequencies. These MLI topologies possess self-voltage balancing of capacitors but more number of power electronic devices are needed.

In this paper, new topology of MLI is presented which possess modular structure as it is connected in a cascaded fashion and provides reliable operation with less voltage stress on the semiconductor switches. It does not require any external circuit for balancing its capacitor voltage due to its self-voltage balancing capability. The proposed topology generate the higher number of output levels with less number of switches and isolated DC sources compared to conventional MLI topologies such as Cascaded H-Bridge MLI, Flying capacitor topology, etc. The number of bidirectional switches also reduces significantly in the proposed topologies. A single-phase Induction Motor acts as load and the speed control is provided by controlling the DC voltage with the help of boost converter which is added between DC source and inverter.

2. Proposed multilevel inverter topology

The proposed multi-level inverter topology consists of seven power electronic switches, two dc voltage sources, ten diodes and a capacitor. The dc Voltage in the right side of load is termed as VSR and the dc voltage source on the left side of load is termed as VSL. The number of levels can be extended by adding more number of cells in cascaded structure.

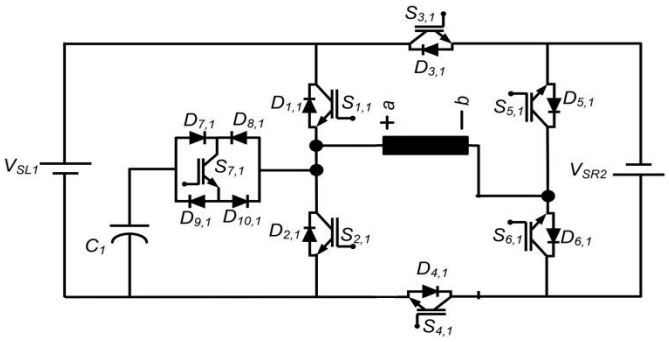

Fig 1 General structure of the proposed MLI

The number of various components required for the proposed inverter for 'N' number of cells are provided with the help of following equations:

DC voltage sources = 2N (1)

Capacitors = N (2)

Power Electronic Switches = 7 × N (3)

Diodes = 10 × N (4)

Output voltage levels = 8 × N + 1

In this, the proposed inverter consists of equal dc voltage sources for each cell. The Table I provides switching sequences for 9-level proposed mli topology along with charging and discharging phenomenon of the capacitor.

TABLE I Switching Table for proposed MLI

S1	S2	S3	S4	S5	S6	S7	Voltage Levels	Capacitor States
0	0	0	1	0	1	1	Vc	Discharging
0	1	0	1	1	0	0	2Vc	No change
0	0	0	1	1	0	1	3Vc	Discharging
1	0	0	1	1	0	0	4Vc	No change
0	1	0	1	0	1	0	Zero	No change
0	0	1	0	1	0	1	-Vc	charging
1	0	1	0	0	1	0	-2Vc	No change
0	0	1	0	0	1	1	-3Vc	Charging
0	1	1	0	0	1	0	-4Vc	No change

From the table I, we can see that the capacitor discharges in the positive half cycle of load current and gets charged during negative cycle of output current. By this, the capacitor gets balanced voltage for each cycle naturally without any control for capacitor voltage balancing.

The operational modes of the proposed mli topology is provided below:

Mode 1:

In this, the switches S4, S6 and S7 are ON. The capacitor C1 will discharge and provide supply to the load. The equivalent circuit for mode 1 operation of proposed mli is provided below:

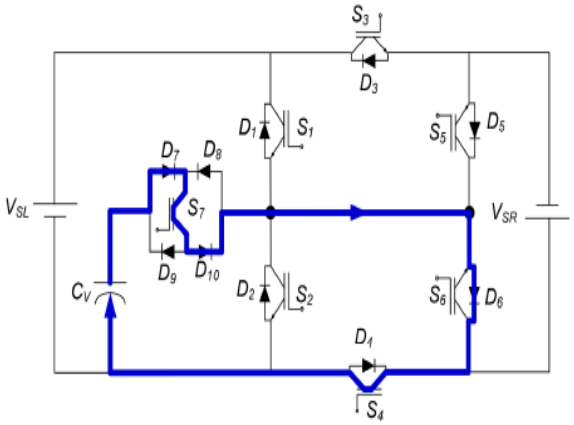

Fig 2. Mode 1 Equivalent Circuit

Mode 2:

In this, the switches S4, S2 and S5 are ON. The voltage source VSR is connected and provide supply to the load. The equivalent circuit for mode 2 operation of proposed mli is provided below:

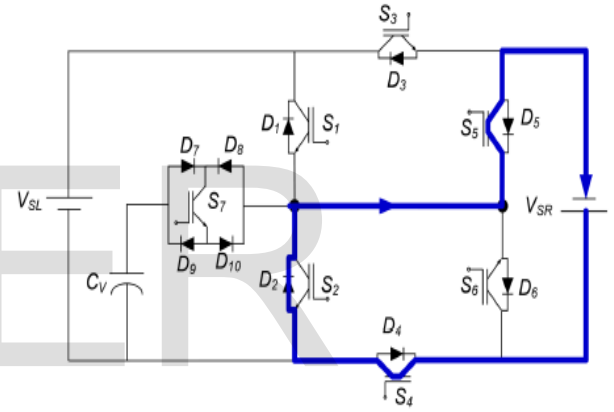

Fig 3. Mode 2 Equivalent Circuit

Mode 3:

In this, the switches S4, S5 and S7 are ON. The capacitor C1 will discharge and provide supply to the load along with the voltage source VSR. The equivalent circuit for mode 3 operation of proposed mli is provided below:

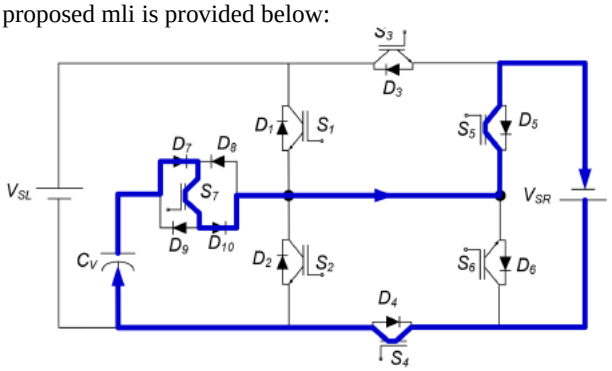

Fig 4. Mode 3 Equivalent Circuit

Mode 4:

In this, the switches S4, S1 and S5 are ON. The voltage sources VSR and VSL combine and provide supply to the load. The equivalent circuit for mode 4 operation of proposed mli is provided below:

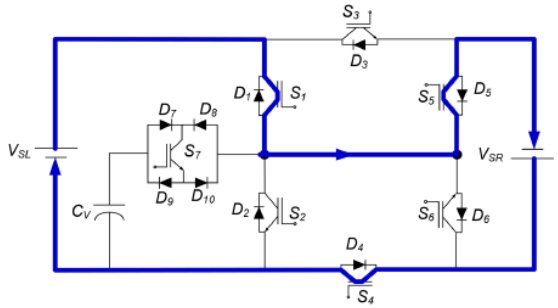

Fig 5. Mode 4 Equivalent Circuit

Mode 5:
In this mode, the switches S4, S2 and S6 are ON. The supply and the load are disconnected in this mode. The voltage across the load is zero. The equivalent circuit for mode 5 operation of the proposed mli is provided below:

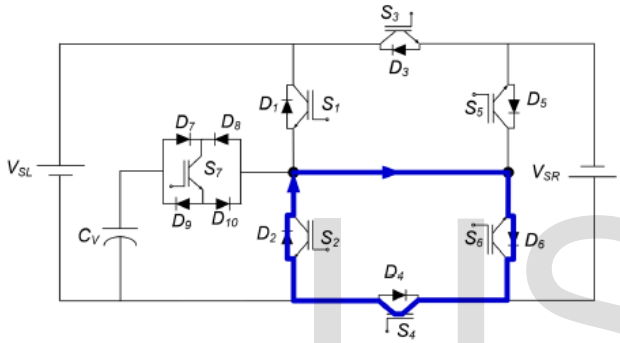

Fig 6. Mode 5 Equivalent Circuit

Mode 6:
In this, the switches S3, S5 and S7 are ON. The capacitor C1 will gets charged and the voltage source VSL provide supply to the load. The equivalent circuit for mode 6 operation of proposed mli is provided below:

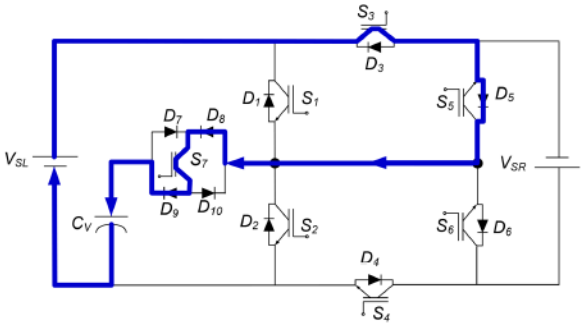

Fig 7. Mode 6 Equivalent Circuit

Mode 7:
In this, the switches S1, S6 and S3 are ON. The voltage source VSL provides supply to the load. The equivalent circuit for mode 7 operation of proposed mli is provided below:

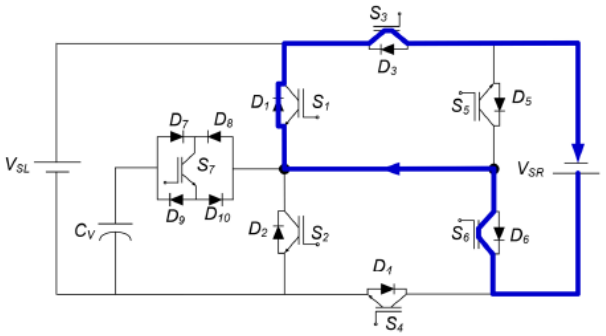

Fig 8. Mode 7 Equivalent Circuit

Mode 8:
In this, the switches S3, S6 and S7 are ON. The capacitor C1 will gets charged and the voltage sources VSL and VSR combines and provide supply to the load. The equivalent circuit for mode 8 operation of proposed mli is provided below:

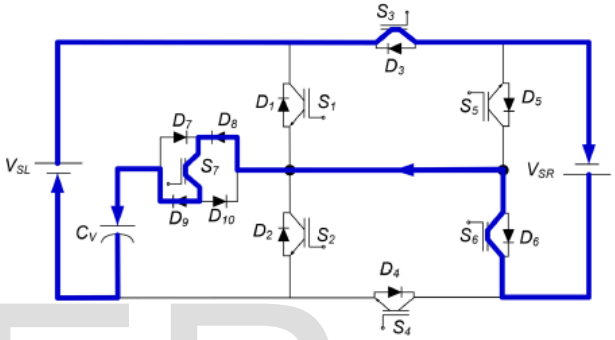

Fig 9. Mode 8 Equivalent Circuit

Mode 9:
In this, the switches S2, S6 and S3 are ON. The voltage sources VSL and VSR provides supply together to the load. The equivalent circuit for mode 9 operation of proposed mli is provided below:

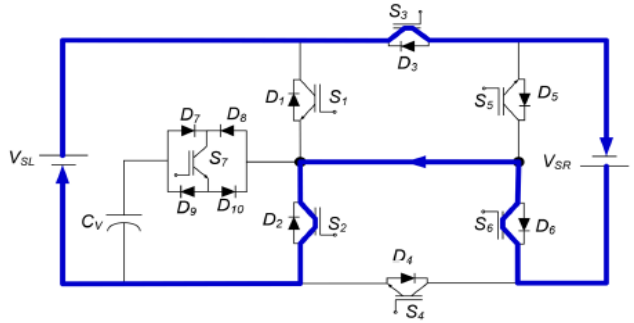

Fig 10. Mode 9 Equivalent Circuit

3. **Boost converter & operational modes**

The configuration of boost converter circuit is provided in Fig. 3 as follows.

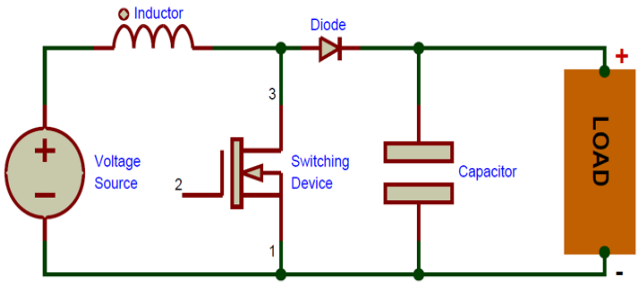

Fig.11. Boost Converter Circuit

The boost converter provides the load voltage higher than that of the source voltage using the pulse width of the gate signals provided for the switch of boost converter. It consists of an switch, inductor, capacitor and diode. The operational modes of the boost converter are provided below:

Mode 1:

The mode 1equivalent circuit of boost converter is given in Fig. 12. Here, switch S is turned ON and the inductor starts to gets charged during this time interval.

The inductor and load voltages are provided below:

$$V_L = V_{in}$$
$$V_{Co} = V_o$$

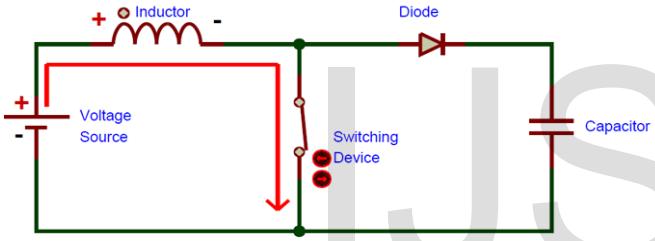

Fig 12 Mode 1, VL=Vin

Mode 2:

The mode 1equivalent circuit of boost converter is given in Fig. 13. Here, switch S is turned OFF and the inductor starts discharging during this time interval.

and connected in series with battery voltage in order to get boosted voltage at load side.

The load voltage are provided in the following equation:

$$V_o = V_L + \hat{V_{in}}$$

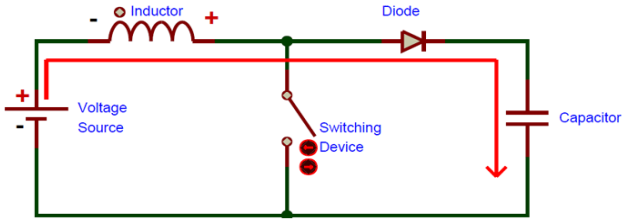

Fig 13 Mode 2, Vo=Vin+VL

Design Procedure of the parameters of Boost Converter:

The circuit parameters of the boost converter are designed using the equations provided below:

The duty ratio of the gate signals provided to the boost converter switch is provided as

$$D = \frac{Vo}{Vo - Vin}$$

The following equation provides the inductor of the boost converter:

$$L = \frac{Vin * D}{\Delta Io * Fsw}$$

The inductor ripple current is determined using the following equation:

$$\Delta I_L = 0.2 * \frac{Vo}{V_{in}} * I_o$$

The output capacitance of the boost converter is provided below:

$$Co = \frac{\Delta Ioc}{8 * Fsw * \Delta Vo}$$

The output capacitor ripple voltage is calculated using following relation:

$$\Delta Voc = 2\% \, of \, Vo$$

4. Control of converter and motor

The Induction motor control along with a boost converter involves two sections such as DC voltage control loop and motor speed control loop.

In this, the generated pulses are provided to the boost converter switch S. The voltage relation is used in voltage control loop in order to control the output voltage of boost converter is shown in figure 14. The reference DC voltage (V^*_{dc}) is as follows:

$$V^*_{dc} = k_v \omega^*$$

The error signal (V_E) from the reference and measured dc voltage is obtained as

$$V_E = V^*_{dc} - V_{dc}$$

The error voltage is generated and provided to proportional–integral (PI) controller, which provides the reference voltage signal V_C as follows

$$V_C(k) = V_C(k-1) + K_P \{V_E(k) - V_E(k-1)\} + K_i V_E(k)$$

where k represents the present instant of sampling. The pulses generated for the boost switch S is of by comparing V_C with high frequency triangular signal M_C as

{If $M_C < V_C$ then the pulse is HIGH}

{If $M_C \geqslant V_C$ then the pulse is LOW}

5. Simulation setup & results

The simulation parameters are provided in the following Table II:

TABLE II SIMULATION PARAMETERS

Parameters	Values

DC-DC CONVERTER	Output Voltage		110 V
	Power		0.5 HP
	BOOST CONVERTER	Inductor	0.34 mH
		Capacitor	552 µF
		Switching Frequency	5 KHz
Battery	Voltage		12 V
	Capacity		15 Ah
Load Arrangements	Voltage		220 V
	Power		0.5 HP
	Frequency		50 Hz
	Rotor speed		157 rad/s

The simulation circuit for proposed nine level mli is provided below:

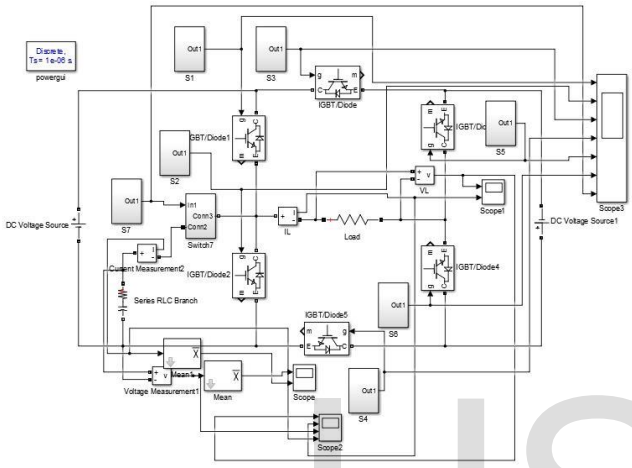

Fig 14 Simulation circuit of proposed nine level inverter

In this, the input voltage for each voltage source is provided as 110V and a resistive load of 370W is provided. The switching pulses for the proposed inverter is provided below:

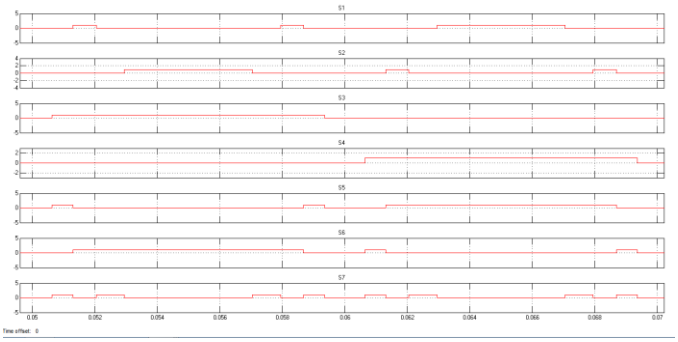

Fig 15 Switching pulses of the proposed nine level inverter

The capacitor charging and discharging characteristics are also provided in the following voltage and current graphs:

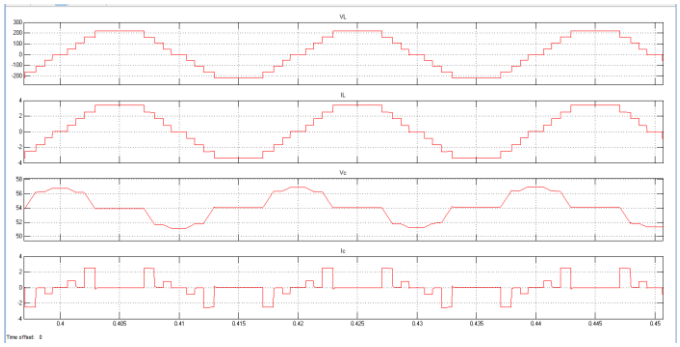

Fig 16 Capacitor voltage and current for charging and discharging characteristics

The simulation circuit for the boost converter fed mli based induction motor drive is provided below:

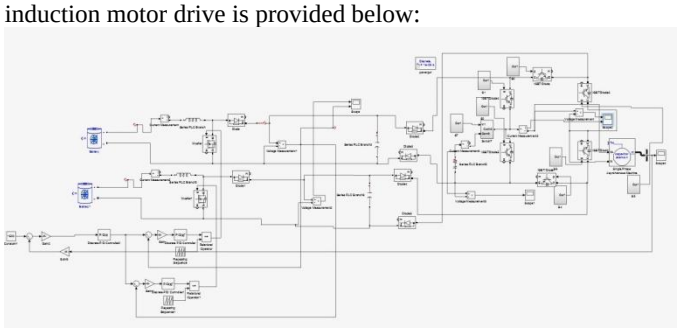

Fig 17 Simulation circuit for boost converter fed nine level inverter based induction motor drive

In this, the boost converter steps up the voltage from battery of 12V to 110V and provided to the inverter. The boost converter operates based on the speed control loop output (Vref) and according to the Vref, the boost converter output voltage will be varied.

The boost converter output voltage is provided in the following graphs:

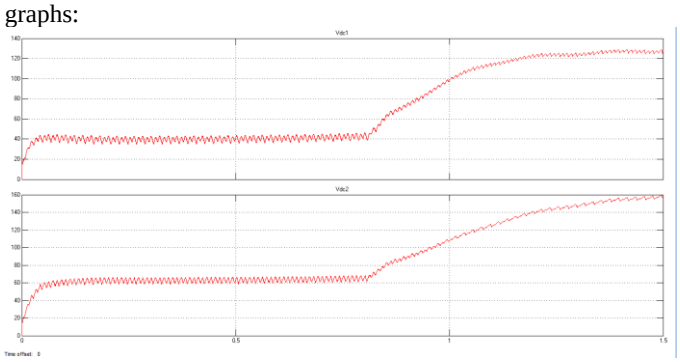

Fig 18 Boost converter output voltage waveforms

In this, the dc voltage is set as 110V based on the reference speed. The rotor speed of the induction motor is provided below:

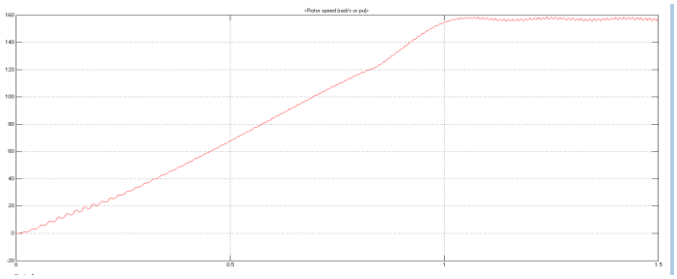

Fig 19 Induction motor speed waveform

The %THD of the proposed multi level inverter is provided in the following graph:

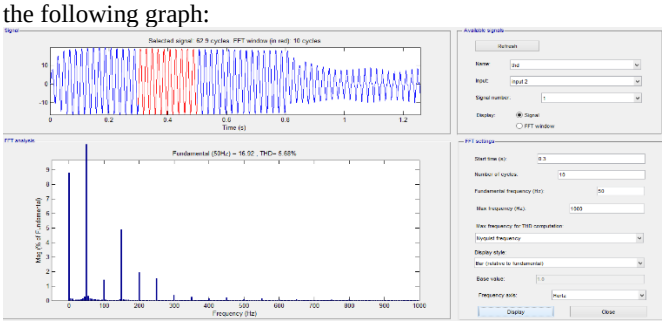

Fig 20 %THD of the load current of proposed mli

In this, the %THD of the load current of proposed nine level inverter is of 5.68%

6. Conclusion

In this paper, a IM drive is designed and simulated with speed controlled by dc voltage control using the boost converter. The dc voltage reference is generated with speed control loop and as the dc voltage is controlled, motor speed is also controlled. The charging and discharging characteristics of the self voltage balancing capacitor is obtained from the simulation work. The switching modes of operation of the proposed inverter is analysed. The harmonic content of the proposed system is measureed from the simulation work.

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